**BITS PILANI, DUBAI CAMPUS**

**DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI**

**FIRST SEMESTER 2023 – 2024**

**COURSE:** CSF303 (Computer Network)

**COMPONENT:** Tutorial Sheet 3 **DATE:** 22nd February 2024

1. Suppose there is exactly one packet switch between a sending host and the receiving host. Assume that the transmission speed of the links between the sending host & the switch, the switch& the receiving host are R1 and R2 respectively. Assuming that the switch uses store-and forward packet switching, what is the total end-to-end delay to send a packet of length L? Ignore, queuing, propagation and processing delays.
2. Consider an application that transmits data at a steady rate (for example, the sender generates an *N-bit unit of data every k time units, where k is small and fixed). Also,* when such an application starts, it will continue running for a relatively long period of time. Answer the following questions. Briefly justifying your answer:
   1. Would a packet-switched network or a circuit-switched network be more appropriate for this application? Why?
   2. Suppose that a packet-switched network is used and the only traffic in this network comes from such applications as described above. Furthermore, assume that the sum of the application data rates is less than the capacities of each and every link. Is some form of congestion control needed? Why?
3. Consider two hosts, A and B, connected by a single link of rate *R* bps. Suppose that the two hosts are separated by ***m*** meters, and suppose the propagation speed along the link is ***s*** meters/sec. Host A is to send a packet of size ***L*** *bits* to Host B.
   1. Ignoring processing and queuing delay, obtain an expression for the end-to-end delay.
   2. Suppose *s=2.5\*10^8 meters/sec*, *L=120 bits*, and *R=56kbps*. Find the distance *m* so that the propagation delay equals transmission delay.
4. Calculate the latency (from first bit sent to last bit received) for:
   1. 10-Mbps Ethernet with a single store-and-forward switch in the path and a packet size of 5000 bits. Assume that each link introduces a propagation delay of 10 μs and that the switch begins retransmitting immediately after it has finished receiving the packet.
   2. Same as (a) but with three switches.
   3. Same as (a), but assume the switch implements “cutthrough” switching; it is able to begin retransmitting the packet after the first 200 bits have been received.
5. The Fig. below shows a multiplexer for Synchronous TDM. Assume that a frame consists of 3 time slots, that each time slot contains 3 bits, and that each frame starts with a framing bit, alternating between 0 and 1. What is the bit sequence on the outgoing link?

